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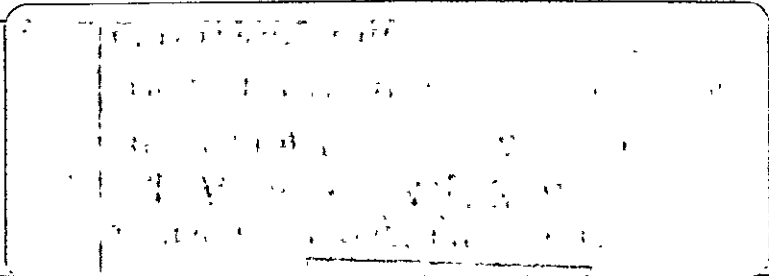
SUMMARY REPORT ON CCD RESEARCH

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16. ABSTRACT  <p>This report summarizes the contractual work on CCD's performed on Contract NAS8-26749. The period of performance covers 1972-1976. First, the fundamental problems encountered in designing, fabricating, and applying CCD's are briefly reviewed. Next the investigations conducted in the contractual work are reviewed and results and conclusions are given. The work is described in four phases which are roughly in chronological order. Phase I deals with the development of design analyses employing computer-aided techniques and their application to the design of a gapped structure. Phase II was concerned with the role of CCD's in applications to electronic functions, in particular, signal processing. Phase III was concerned with extending the CCD to materials other than bulk single crystal silicon. The material used was silicon films on sapphire (SOS). Phase IV has dealt with all aluminum transfer structure with low noise input-output circuits. Finally, a brief review of related work done by the contractor on CCD imaging devices is given.</p>			
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## INTRODUCTION

The following summary is best placed in perspective by reviewing the approach and objectives as outlined in the scope of work. The first objective has been to attempt to sense the directions of development in the CCD field by a continuous survey of the literature (trends approach.) The second objective has been to identify special problems of potential significance and investigate them in detail.

This work has dealt with the development of analytical and design techniques and application of them to novel CCD structures. (Techniques approach.) Therefore, the contractual work done has been close to the mainstream of CCD research, and it is easy to simultaneously summarize the overall development in the field while reviewing the contractual work.

With the benefit of six years of hindsight some general observations can be made, which are useful in evaluating progress in the field. First, essentially all of the physical theory of MIS structures was available before the advent of the CCD. It is quite clear that the implications of the theory were not understood and that the development of CCD's has dramatically sharpened the understanding of those implications. Early reports<sup>1,2,3</sup> of the CCD as a "junctionless" device raised many hopes for fabrication of CCD's on materials other than silicon which have not been realized and will not likely be realized in the near future. Second, the CCD is a "two-dimensional" (at least) device that requires more than a simple one-dimensional electric field analysis in general. The MOS transistor can be treated

quite effectively by a one-dimensional analysis extended by the "gradual channel" approximation. This device and the MOS capacitor were the vehicles for testing MOS theory prior to the CCD invention. A one-dimensional analysis of a CCD structure is invaluable, but it is quite incomplete. Much of the developmental progress for CCD's has resulted from better understanding of the nature of the "two-dimensional" fields and of the proper application of one-dimensional type analysis in the design of the CCD. In summary, the CCD is a much more complex device than many originally assumed it to be. Its operation is more subtle, there are many critical operational parameters, and the process for producing a successful CCD is much more complicated than it first appeared to be. Consequently, there has been a wealth of problems requiring solutions. Much progress has been made, but, if many of the originally hoped for applications of CCD's are to be realized, there are many problems remaining to be solved.

The problem areas are described briefly in the following and will be discussed in more depth later in the summary of the contractual work which has dealt with almost all these areas.

#### A. The Charge-Up Time<sup>4</sup>

It is axiomatic that charge can be transferred from the well under one electrode to that under an adjacent one within a certain transfer time,  $\tau_T$ . The fraction of the charge remaining in the originating well decays roughly exponentially with time. During the time for transfer and in the intervening interval before transfer is made possible, thermally generated carriers are collected in the well.

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The accumulated charge due to this thermal source must be small compared with the signal charge or the well is filled and overflows, or otherwise the dynamic range for signal charge is reduced. Bulk silicon with a thermal oxide operates so well in this regard that the problem is usually ignored for that case. For materials other than bulk silicon the problem is significant and limiting. This problem is quite significant in the contractual work on SOS devices.

#### B. The Inter-Electrode Barrier Problem<sup>3,5</sup>

This problem was one of the earliest to be recognized for CCD's, and the solutions proposed to date have resulted in vastly increased complexity of the CCD structure. Briefly, if two transfer electrodes are separated by a distance exceeding the depletion depth, an electrostatic barrier forms between the electrodes precluding complete charge transfer. A number of solutions have been offered which reduce in principle to: (1) use of overlapping transfer electrodes, (2) doping in the gap for control of the gap surface potential; (3) conductively coupled transfer electrodes by doping patterns in poly silicon. The earliest work<sup>6,7,8</sup> in this contract dealt with analysis of the two-dimensional fields using computer techniques and with applications of the techniques to the evaluation of proposed solutions (1) and (2) above to the problem. Solution (3) is successfully used to fabricate imaging devices commercially available, but this was not studied.

#### C. The Transit Time Problem<sup>9,10,11</sup>

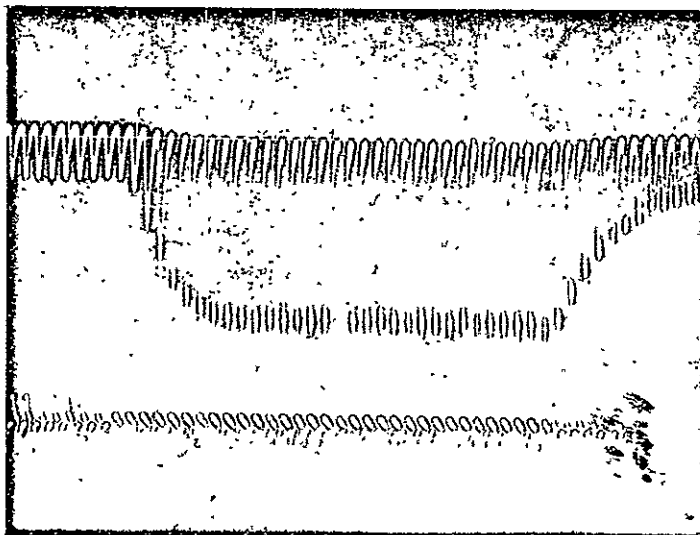
The transfer of charge between two electrodes is governed by diffusion and drift mechanisms. The slowest possible transfer occurs

when carriers migrate due to diffusion only, in which case the transfer time depends proportionally upon the square of the transfer electrode width. Therefore, narrow electrodes, i.e. small bit cells, result in increased operational speed. In addition to minimizing the geometry, the speed may be enhanced by designs which result in an aiding lateral electric field under the transfer electrodes, thereby increasing the velocity of the charge being transferred. The "buried-channel"<sup>26</sup> or "peristaltic"<sup>27</sup> CCD structure realizes this advantage by pushing the signal charge away from the silicon-SiO<sub>2</sub> interface into a region of increased fringing field. Earlier contractual work dealt with the problem of charge-transfer dynamics analyzed by computer aided techniques.<sup>10</sup>

#### D. The Interface State Problem<sup>12</sup>

It has long been recognized that the discontinuity of a semiconductor at an interface introduces charge states within the band-gap. When an SiO<sub>2</sub> layer is grown or deposited on silicon, it is possible for fixed charges to exist within the oxide thus increasing the number of available states, which are accessible, in this case, by tunneling into the oxide. Typically, the occupancy of these states are ignored except for analysis of noise, and their effect enters through a space charge mechanism only. Each state has a lifetime; generally levels close to the band edge have the shortest lifetime and deeper lying states have longer lifetimes. The short lifetime and long lifetime states are referred to respectively as "fast" and "slow" surface states. This phenomena is important for several reasons: (1) charge in these states regulates the electrode voltage at which signal charge can be controlled, i.e. the threshold.





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Figure 1

Pulse Train Response For 32 Bit CCD on SOS  
 Showing the Effect of Charge Transfer Efficiency  
 in Delaying the Rise and Fall of the Output.

Top Trace: Output Diode Signal, 0.5 V/cm.  
 Bottom Trace: Input Diode Signal, 0.2 V/cm.  
 Horizontal: 50  $\mu$ Sec/cm.

(2) Signal charge will be trapped upon transfer to a well with an abundance of empty surface states. This charge will not be totally released during the subsequent transfer operation but will be released later. This results in a charge transfer inefficiency on a dynamic basis, the ultimate effect of which is dispersive type distortion for delay line operation. That is, a train of pulses will not be faithfully reproduced at the output, rather the first pulses are attenuated and a trailing group of pulses is observed after the train should be complete, as is illustrated in Figure I. (3) The random trapping and release of charge results in noise at the output. This noise may significantly reduce the sensitivity of the CCD for low-level signal applications.

Two solutions to this problem are the "buried-layer" structure<sup>26,27</sup> and the use of a bias charge or "fat zero." Earlier work<sup>8</sup> on analysis programs and later work<sup>13</sup> on the CCD's on SOS have dealt with this problem. For CCD's on SOS the interface between the silicon and sapphire is particularly important because of the "charge-up" time problem and the noise problem.

#### E. Structural Difficulties and Limitations.

Solutions to the preceding enumerated problems have resulted in more complex structures than originally thought to be necessary. Some are trivial in complexity for application to bulk silicon devices, i.e., techniques such as multiple input and output gates, floating diffusion and floating gate output sensors. The use of overlapping electrodes requires the presence of an insulator that can be produced by a fabrication process compatible with the overall technology.

Two techniques have been proposed; (1) silicon-aluminum gate structures insulated by  $\text{SiO}_2$ , and (2) aluminum gates insulated by anodic  $\text{Al}_2\text{O}_3$ .<sup>14</sup> The former technique enjoys a proven reliability record in MOS integrated circuit technology. The long transmission line resulting from an all poly-silicon construction has excessive delay for very high frequency applications. Furthermore, the poly-silicon gate, though very well understood and executed by the leading technologists, is an undesirable complication from the viewpoint of many. The anodized aluminum gate structure has the advantage of high conductivity, thus reducing undesired delay distortion, and is relatively simple compared to the poly-silicon gate technology. It does not have a reliability track record. Later phases of the contract work have dealt with both of these technologies, especially with the anodized aluminum structure. Both of these solutions to the interelectrode gap problem create difficulties for application of imaging devices, a subject addressed in the contractual work on CCD's on SOS.

The solution to the interelectrode barrier problem by doping the gap raises two problems. First, and simplest, is that reasonable solutions require doping by shallow ion-implanted layers. This is trivial except that it adds a process step and requires an ion implanter. Second, not all of the proposed techniques work, and those which do also introduce speed limitations which were not originally recognized. The contractual work has investigated the use of uniform doping which can be effectively realized by control of the surface state charge and which, unfortunately, does not work well for reasons which were not originally obvious. The use of selective implantation between electrodes produces workable devices with speed limitations as discussed later. Contractual work on the two-

dimensional analysis of CCDs has produced some valuable insight into these problems.

#### F. Applications of CCDs

The viability of the CCD in applications depends upon how well it performs electronic functions as compared with competitive devices. The contractual work in this area has been only of a survey nature with respect to memories; however, some original work has been done with respect to signal processing and some related work was done on imaging devices supported elsewhere. (MICOM)

##### 1. Memory:

The CCD is well suited for dynamic memories which are serially organized. The advantage of the CCD with respect to most semiconductor memories has been in bit density and simplicity of fabrication. At this time, simple MOST memories with one transistor memory cells are competing very favorably with respect to bit density. Magnetic bubble memories are very dense and nonvolatile; however, there are differences of opinion as to the ultimate practicality of manufacture and operation of these devices.

##### 2. Analog Signal Processing:

Activities in this area have been most symbolic of the high hopes for the CCD. The concept of "optimal filtering" of signals on a real time basis has been slow to materialize because of the complexity of the hardware required for realizing complicated transfer functions. For many years the concept of a tapped delay line with variable tap weights and a summing

network has been appealing for realizing transversal-type filters. Variations incorporating feedback allow recursive filter designs. At present, fully digital filters which use A/D and D/A conversion in conjunction with digital computation and data handling allow "optimal filtering" for low frequency signals in real time. The barrier to penetration into this area of application by the CCD is the successful implementation of taps. To date, only rather inflexible and moderately accurate schemes<sup>15</sup> or schemes that are of unproven reliability have been implemented.<sup>16</sup> The surface charge transistor structure appears to have a practical implementation advantage.<sup>17</sup>

The contractural work has investigated the use of delay lines in serial-type data processors.<sup>18</sup> For moderately low frequencies, ordinary untapped CCD's can be used for "close to optimal" filtering.

### 3. Imaging<sup>19</sup>

In this area, the CCD compares quite favorably with competing solid state devices as is evidenced by the emergence of the first commercially available CCD as a camera element. The CCD operation is a natural serial mode suited for TV-type scans. Partial field scans are more difficult than for the CID. The CCD is more difficult to protect from blooming phenomena than are the CID or photo transistor array imagers. In terms of element density, resolution, dynamic range, and spectral selectivity, the CCD compares favorably with the other

silicon devices. The field has matured to the point that certain CCD implementation schemes are now identifiable as superior. However, there is room for improvement with respect to sensitivity, spectral selectivity, and frame rate. The use of materials other than silicon lies further on the horizon awaiting solution of the previously described problems.

In the following, five detailed summaries are given for contractual and related work which was performed in overlapping phases which are described in an approximately chronological sequence.

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# PHASE I ANALYSIS AND DESIGN PROCEDURES<sup>6,8</sup>

This work was begun in 1972 at which time there was very little published material on two-dimensional analysis of CCD structures, and there was a great deal of conflicting opinion concerning the optimal solution of the inter-electrode barrier problem. Although the concept of overlapping poly-silicon and aluminum electrodes was being explored, there was a great deal of interest in gapped structures. The gapped structure was especially attractive for imaging applications because photons are received almost unobstructed in the gap. All schemes for using a gapped CCD structure rely upon doping in the gap and, possibly, beneath the electrode edges. One dimensional analysis for such schemes is invaluable and imperative; however, such an analysis is at the same time inadequate for a complete assessment of the feasibility of the design. This is best illustrated by a concrete example which was studied in the contractual work.

Doping is required in the gap to establish the surface potential so that no barrier can form. Consider the N-channel CCD illustrated in Figure 2. Within the gap region, (and possibly under the electrodes) there is a shallow N-doped layer yielding a positive fixed charge which tends to drive the surface potential positive. Defining the fixed charge as  $Q_F$  and the mobile electron charge as  $Q_n$ , the surface potential in the gap is:

$$\psi_s = (Q_F - Q_n)^2 / 2\epsilon_s q N_a \quad (1)$$

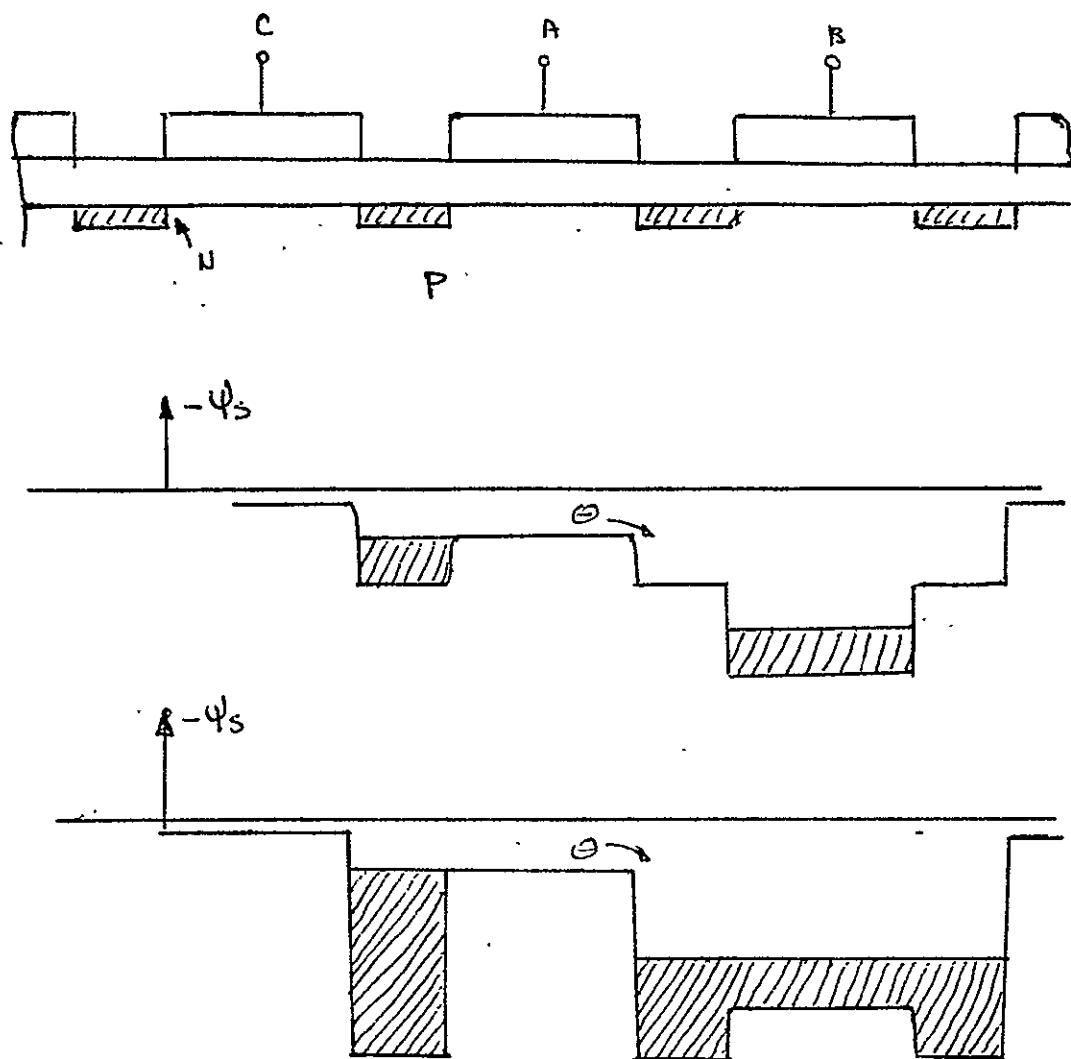


FIGURE 2

Surface Potential Profiles For a  
CCD With Shallow Gap Doping

- (A) Transfer Gap Depleted.
- (B) Transfer Gap Accumulated.



Where  $\epsilon_s$ ,  $q$  and  $N_a$  are respectively the substrate permittivity, electronic charge, and substrate doping density. Within the gap  $Q_F$  results from a thin layer of N-type dopant and the Si-SiO<sub>2</sub> surface state charge. Beneath the electrodes the surface potential may be calculated from:

$$\psi_s = V_G' + V_1 - \sqrt{V_1^2 + 2V_1 V_G'} \quad (a) \quad (2)$$

$$V_G' = V_G - V_{FB} - Q_n / C_{ox} \quad (b)$$

$$V_1 = q N_a \epsilon_s / C_{ox}^2 \quad (c)$$

Where  $V_G$ ,  $V_{FB}$  and  $C_{ox}$  are respectively the gate voltage, the flat band voltage including the effects of all fixed charge, and the oxide capacitance. The surface potential both beneath the electrode and in the gap has a maximum value for  $Q_n = 0$ , i.e. a depleted condition. There are two possible situations depending upon the magnitude of  $Q_F$  and the electrode bias, which are illustrated in Figure 2. In Figure (2.a), the adjacent electrode voltage pulls the surface potential to a value exceeding the maximum for the gap as obtained by (1). If the left hand electrode is at a still lower potential, charge is transferred left to right. In (2.b), the right hand electrode produces a surface potential inadequate to deplete the gap region. Therefore, the gap surface potential floats at the adjacent level with free charge remaining along the surface in the gap. Again, if the left hand electrode is at a lower potential, charge transfers left to right.

The former scheme is attractive because it appears that no ion-implantation is required, rather the fixed charge can be the surface state charge which is controllable by well-known process steps. Such a scheme has been proposed<sup>20</sup> and was the subject of investigation in this work.<sup>6,8</sup> The investigation proceeded along both experimental and theoretical lines as described.

The theoretical work consisted of the development of several computer programs which are applicable to this and other problems.<sup>8</sup> The programs utilized the successive-over-relaxation algorithm to obtain two-dimensional electrostatic analyses and used implicit integration schemes to study the dynamics of charge transfer.<sup>6,10</sup> The latter work on charge transfer dynamics was similar to work of others which was later published.<sup>11</sup> The electrostatic analysis was based upon a general depletion model in which the minority carrier density is assumed to be zero. Several factors which influence the non-linear analysis of the fields were investigated. These factors included: (1) the grid-size distribution influence on accuracy and computational speed; (2) the rate of convergence with iteration number as affected by the relaxation parameter; (3) the method for treating the non-linear dependence of the space charge density upon the potential field; (4) the effect of starting solution approximations on convergence. A novel feature of the programs was that they were formulated on a Gauss's law model rather than the Poisson's equation<sup>5</sup> which made the boundary conditions for rather complex structures easy to program. Figure 3 shows the results for the CCD geometry which was used for the experimental device although all parameters do not correspond. The results of a one-dimensional analysis are also included in Figure 3.

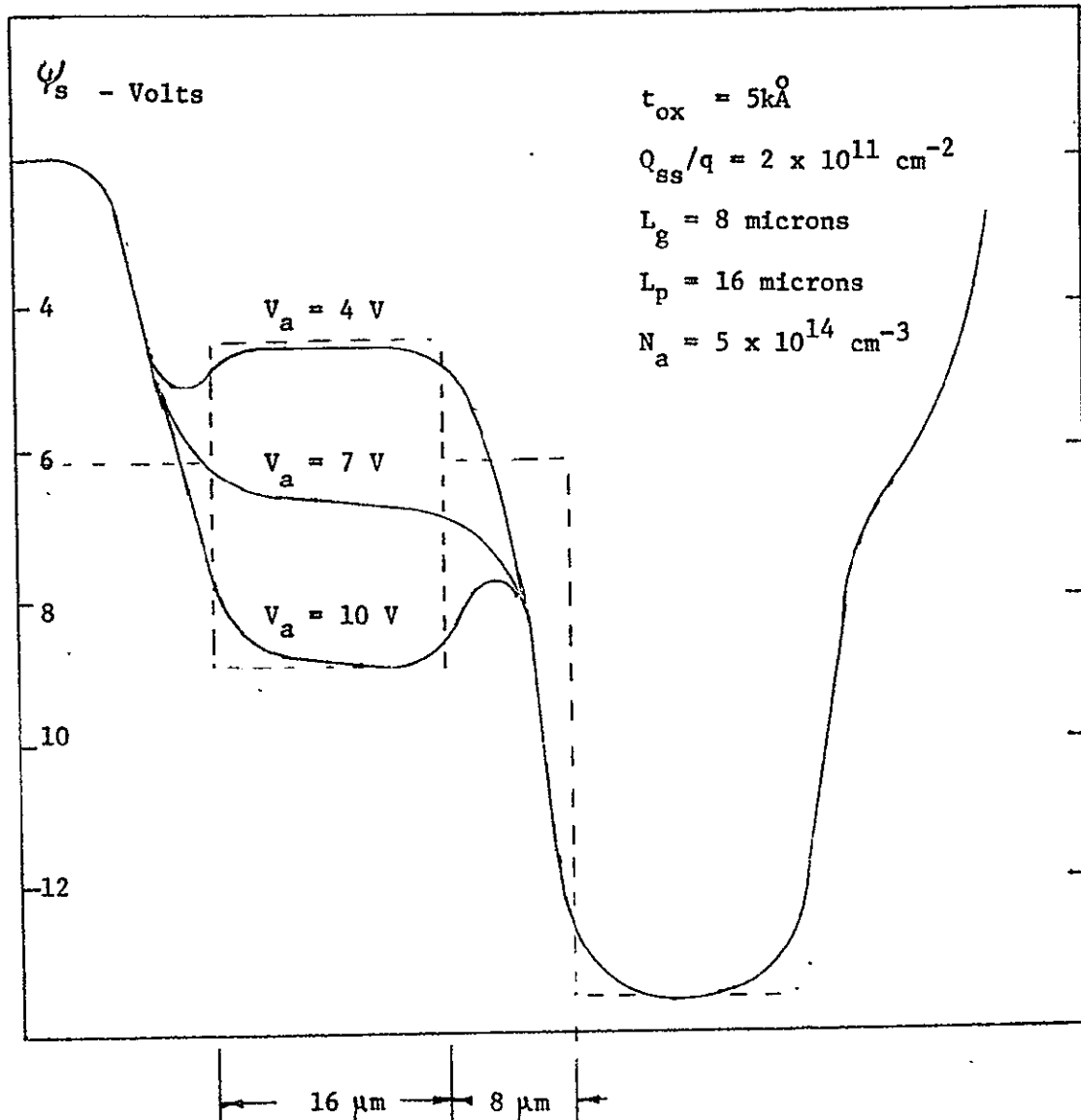


FIGURE 3

Calculated surface potential profiles from a 2-dimensional, numerical analysis of CCD structure.<sup>8</sup>  
 Dotted lines give results of 1-dimensional analysis.

Figure 4 shows the results for charge transfer dynamics for a typical fringing field on the order of 100v/cm at the center of an electrode. This plot of transfer inefficiency vs. normalized time is not greatly different from earlier work<sup>9</sup> showing that diffusion plays a large role in the transfer process. A tolerable inefficiency of  $\epsilon = 10^{-3}$  for a short shift register (16 bits) requires a time  $t \geq 10W^2/\mu$  where  $W$  is the pad width and  $\mu$  is the mobility. For  $W = 16 \mu\text{m}$ ,  $\mu = 200 \text{ cm}^2/\text{Vs}$ ,  $t = 0.13 \mu\text{s}$ . The maximum frequency of operation for this condition is  $f = (1/3) (1/.13)$ , or  $f = 2.5 \text{ MHz}$  for a 3-phase device.

The preceding analysis, although much more thorough than a one-dimensional approach, is also incomplete. The free-charge has a strong influence upon the field which is not included. A comprehensive two-dimensional approach is required; however, it was soon determined that the computational time required for such an approach quite clearly was too expensive to remain within the scope of the effort. Other researchers have since reported similar conclusions in their own work<sup>21</sup>. In fact, there is some doubt that such an approach will ever be used as a design procedure.

Simultaneous with the analytical approach, an experimental device was constructed which was a 16 bit, 3-phase N-channel device. The objective was to keep the fabrication procedure as simple as possible. Two parameters were released because of expediency: (1) the P-substrates were doped an order of magnitude higher than desired, (2) the oxide was 1200Å rather than 3,000-5,000Å. Time and equipment limitations precluded obtaining these parameters. Flat band voltages after sintering, but without annealing, gave  $Q_{ss}/q = 1.3 \times 10^{11} \text{ cm}^{-2}$ , lower

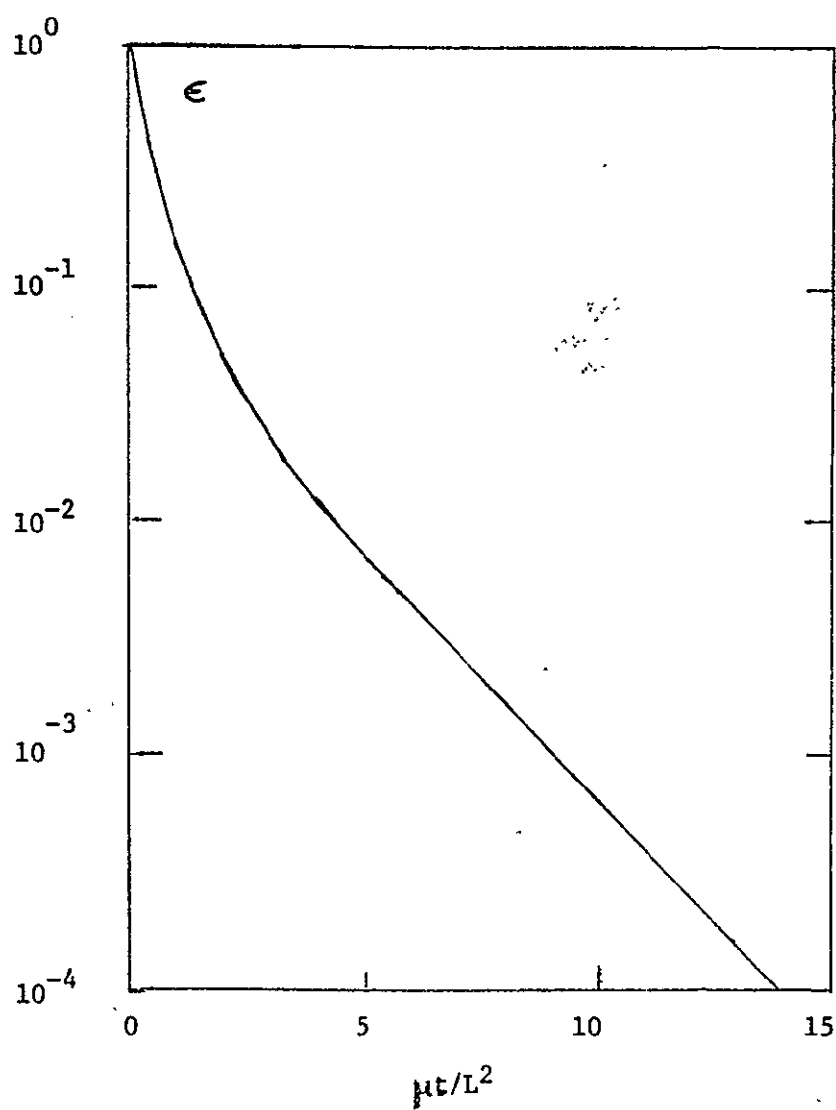
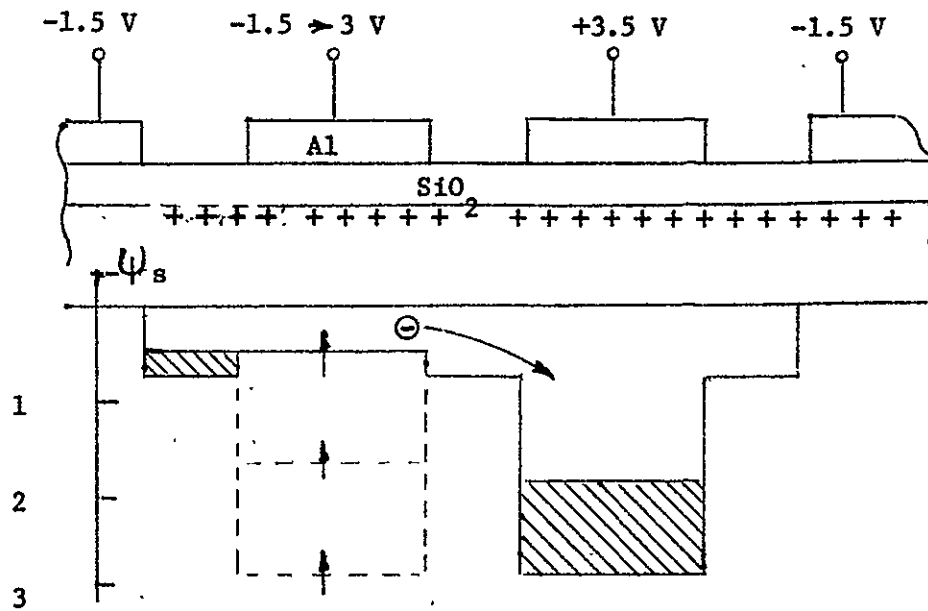


FIGURE 4

Typical charge transfer inefficiency dependence upon the normalized transfer time, reference 11.



$$t_{\text{ox}} = 1200 \text{ \AA}$$

$$N_a = 3.8 \times 10^{15} \text{ cm}^{-3}$$

$$Q_{\text{ss}}/q = 1.3 \times 10^{11} \text{ cm}^{-2}$$

$$L_p = 0.6 \text{ mils}, L_g = 0.3 \text{ mils.}$$

FIGURE 5

Surface potential profile for 3-phase CCD from one-dimensional analysis.

than anticipated. With  $N_a = 3.8 \times 10^{15} \text{ cm}^{-3}$ , the calculated gap potential is  $\psi_s = 0.35\text{V}$ . Under the electrode, the surface potential is:

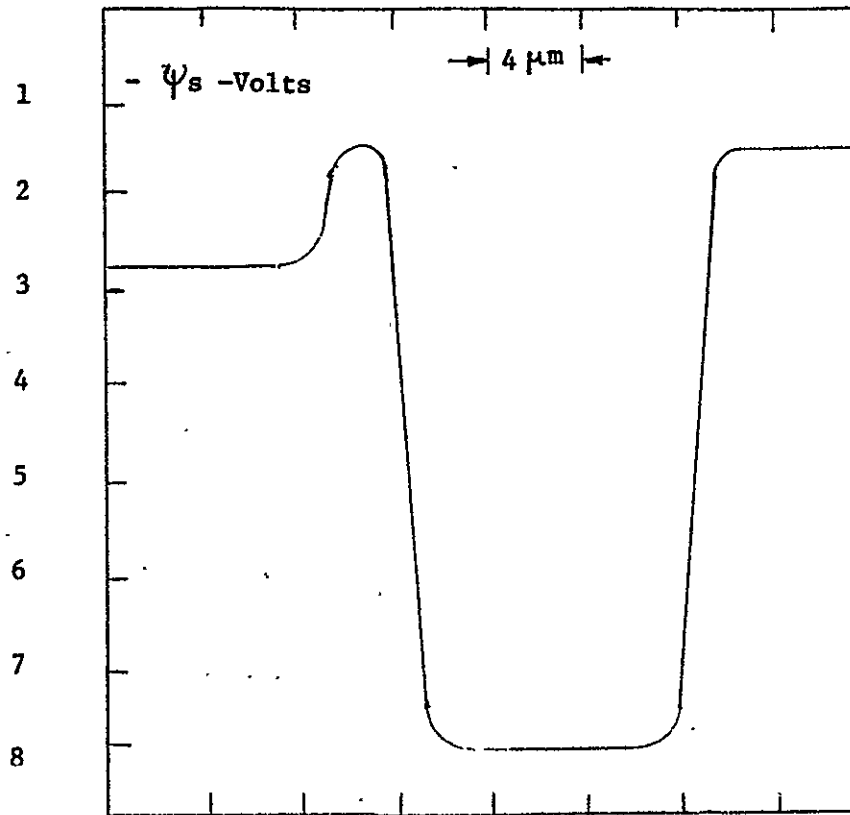
$$\psi_s = V_G + 2.36 - \sqrt{1.52V_G + 3.01} \text{ Volts}$$

Giving  $\psi_s \approx 0$  at  $V_G = 1.5\text{V}$ ,  $\psi_s = 2.97\text{V}$  at  $V_G = +3.5\text{V}$ .

Therefore, the device should work with a 5 volt clock swing and 1.5V substrate bias. Figure 5 indicates the surface potential profile for the device from the one-dimensional analysis.

A three-phase test circuit was built<sup>20</sup> and the devices were tested both dynamically and by curve tracer methods. The results indicated that the devices should transfer charge; however, dynamic operation was unsuccessful. Two unanticipated problems were identified: (1) the leakage current was so high that the output diode was insensitive. (2) the CCD pulser did not have sufficient control on the overlap and trailing edge response. The first problem could be cured by a P+ guard band diffusion. The second problem existed only because of the poor CCD response. The other problems resulted from lack of control over parameters. The substrate doping was too heavy which reduced the gap potential achievable under depletion. The oxide thickness was too thin, thus, reducing the fringing field, especially in the critical gap area, which increased the transit time. Figure 6 shows the results for a computed profile with a thin oxide. All of these problems could be corrected to produce a workable device; however, the two-dimensional analysis reveals a fundamental problem which significantly limits the overall approach as discussed in the following.

In figure 3 (and 5) it is evident that the gap doping results in a well to the left of the transferring electrode. Therefore, some charge is always pumped backward resulting in a loss of efficiency.



$$t_{ox} = 1000 \text{ \AA}$$

$$N_a = 1 \times 10^{15} \text{ cm}^{-3}$$

$$Q_{ss}/q = 6 \times 10^{11} \text{ cm}^{-2}$$

FIGURE 6

Surface potential profile for CCD with thin oxide showing the reduced fringing effect with respect to the thicker oxide case in Figure 3. (Reference 6.)



This same problem occurs even if the gap is doped heavy enough to preclude depletion in the gap. The loss in transfer efficiency also reduces the speed of operation as expressed by the modulation transfer function, MTF, given by:<sup>22</sup>

$$MTF = \exp \left\{ -N\epsilon \left[ 1 - \cos(\pi f/f_m) \right] \right\}, \quad (3)$$

where  $N$  is the number of transfers in a shift register,  $\epsilon$  is the charge transfer inefficiency,  $f$  is the frequency of an input sinusoidal signal, and  $f_m$  is the Nyquist (half of the clock) frequency. Therefore, the attenuation for a sinusoidal input signal at a fixed frequency and fixed shift register length increases exponentially with the charge transfer inefficiency. Later attempts to extend the above scheme by heavier gap doping and enhancement doping under the electrode edges for a unidirectional two-phase device confirmed this reduction in speed.<sup>23</sup> Others<sup>24</sup> have discussed the dilemma emphasizing the increase in  $\epsilon$  at high signal levels; however, the phenomena holds at low levels as well. It appears that any scheme for gap doping results in a device with lower transfer efficiency and operating speed than can be achieved with overlapping structures. This result is well known for the bucket brigade device (BBD), and one may note that the structure corresponding to Figure (2-b) can very well be considered to be a self-aligned gate BBD.

Toward the end of 1973, it was decided to discontinue this approach utilizing gapped structures. It was clear that workable schemes required more complex CCD structures than originally envisioned. It was also clear that gapped devices would not perform as well as gapless devices.

Furthermore, devices with the channel oxide covered by a conductor are more stable over a period of time because they are not affected by the accumulation of static charge on the insulator over the channel. There were many reports in the literature which agreed with these conclusions although work was continuing on gapped devices at some laboratories.

## PHASE II CCD APPLICATIONS<sup>18,25</sup>

This work overlapped that of Phases I and III and investigated the applicability of CCDs to analog signal processing. It was quite obvious that many difficulties precluded the immediate use of CCDs for realizing complex filter functions. The main problem is in tapping a CCD delay line. A simple but elegant tapping concept has been developed Texas Instruments researchers<sup>15</sup>, but it was apparent that the scheme would be very flexible, that accuracy would be limited, and that the fabrication procedure was not trivial. Their scheme involved splitting the transfer electrodes and sensing the charging current. Other schemes later<sup>16</sup> also had limitations due to complexity, both with respect to fabrication and operation. These schemes utilized MNOS transistors for obtaining variable tap weights with memory. The contractual work developed a little known scheme which can use an ordinary digital delay line to implement an analog signal processor as described in the following.

The processor is referred to as a DELTIC DFPCC, where DELTIC stands for delay line time compression and DFPCC stands for difference frequency polarity coincident correlator. Figure 7 illustrates the principles of operation which work effectively for signals with information coded into the zero crossings. The input circuit rejects out of band noise and clips the remaining signal plus noise. This composite is then heterodyned down close to base band, filtered by a unique low pass

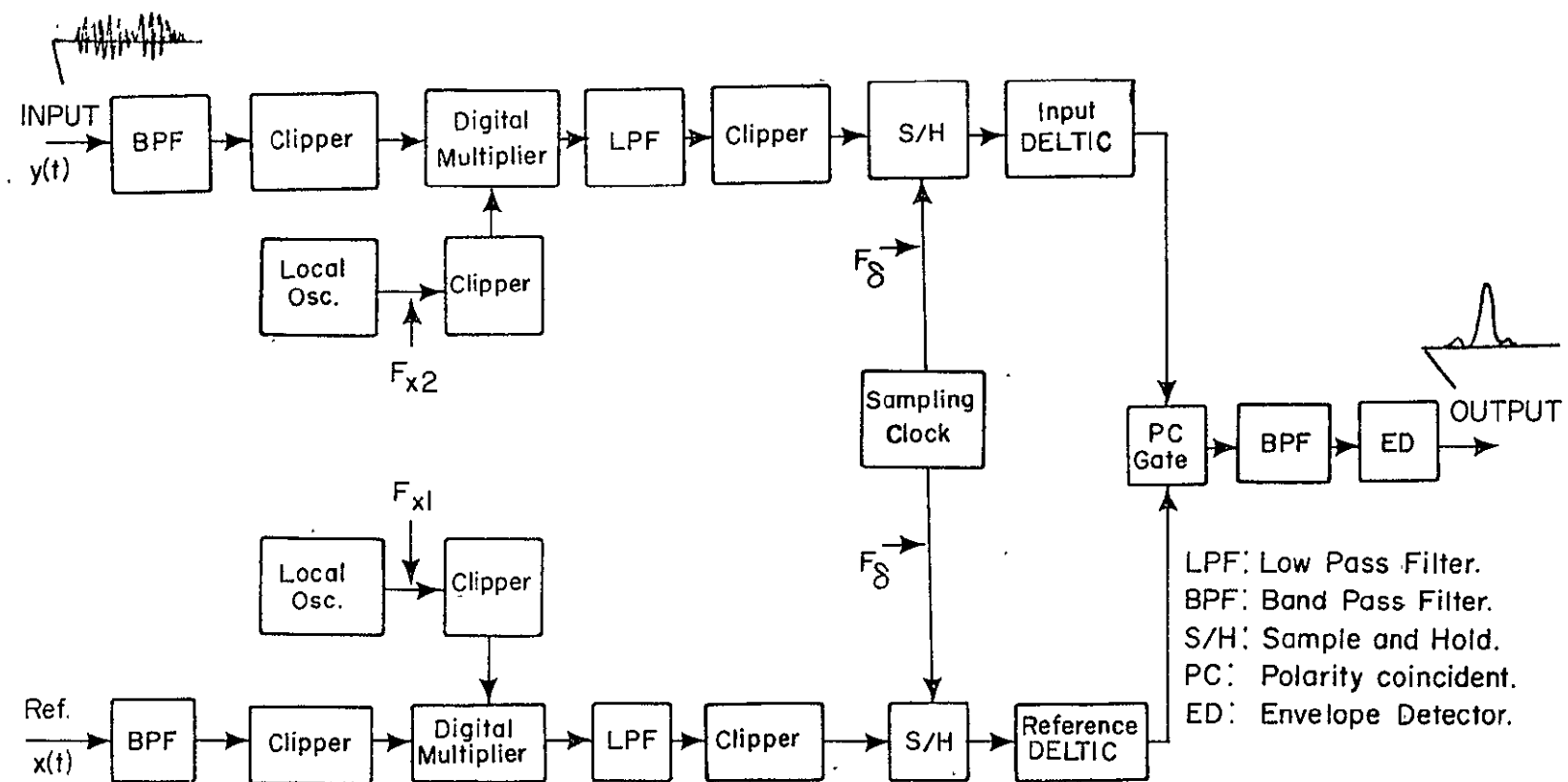


Figure 7 Block Diagram of DELTIC DFPC Signal Processor.<sup>18</sup>  
 See Reference 18 for full discussion.

and loaded into a recirculating memory, which is the DELTIC. A similar operation is performed on the reference signal, which typically would be the waveform for an undistorted received signal for an ideal situation. The band edges for the signals in the two DELTICS are slightly different so that the product of the two signals yields a difference frequency, the objective of which is to eliminate fading in a practical system in which the carrier phase may vary in random fashion. The output of the DELTIC product is filtered by an interpolating band pass filter and detected by an envelope detector. The final output is a correlation spike with some background noise. Signal to noise ratio improvement by over 20 dB was obtained.

The contractual work extended the theory of operation for such a processor, developed a theoretical design procedure, developed circuit design schemes for more fully exploiting LSI digital techniques for implementation, and resulted in an experimental breadboard system. Tests results from the breadboard system corroborated the new theoretical result. The conclusion from this phase of the work was that it is immediately practical to construct a sophisticated serial type signal processor using CCDs as well as other LSI structures for processing audio bandwidth signals. The most obvious application for the CCD is for the DELTIC; however, other circuits in the processor such as the LPF can utilize simple CCD structures. As high frequency CCDs<sup>26,27</sup> become available, the bandwidth which can be handled will be increased.

Also as part of this work, the relative merits of serial and parallel type signal processors were compared, and the various schemes for building parallel type processors were studied. It was quite clear from a review of the literature that frequency modulated signals,

such as the DELTIC DFPCC is applicable to, are of the greatest interest. Some of the processing schemes reviewed utilize clipping as required for the DELTIC DFPCC system. It is quite clear that parallel signal processors such as the "matched" transversal filter as implemented by CCDs face difficult practical problems. Of the various LSI schemes which have been proposed, the scheme proposed by General Electric which uses the surface charge transistor (SCT) concept appears to be most promising.<sup>17</sup> The similarity between the SCT and the CID imaging device, both GE concepts, is interesting and both compete with CCDs in applications.

### PHASE III CCDs ON SOS (Silicon on Sapphire)

Although CCDs on SOS are feasible, there are inherent problems, some obvious, requiring further research before they can be widely used. There were three reasons initially why the project of developing CCDs on SOS was of interest. (1) There is a strong interest in extending CCD technology to materials other than bulk silicon in order to benefit from unique features such as spectral selectivity, higher mobility, etc. Many of the problems encountered in building CCDs on SOS are similar to those for other materials; however, SOS is better understood in many respects and more easily processed. (2) The computer analyses of CCDs done in Phase I indicated that the fringing field is stronger in a depleted SOS film and the operational speed should be ultimately higher than for surface channel devices on bulk silicon. (3) The use of back side imaging through the transparent sapphire substrate suggest possible advantages. This project was carried out in collaboration with Dr. D. Kranzer, an NRC Fellow (1973-1975) at Marshall Space Flight Center.

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The first problem was that the charge-up time for CCD's on SOS could result in significant limitation for the minimum operating frequency. The charge-up time,  $T_c$ , for an MOS capacitor on bulk silicon with uniform substrate doping,  $N_B$  and lifetime,  $\tau$  is:<sup>4</sup>

$$T_c = 2 \left( \frac{N_B \tau}{n_i} \right) \left\{ C_{ox} \left( \frac{W_0 - W}{\epsilon_{si}} \right) + \left( C_{ox} \frac{W_f}{\epsilon_{si}} + 1 \right) \ln \left( \frac{W_0 - W_f}{W - W_f} \right) \right\} \quad (4)$$

Where  $n_i$  is the intrinsic carrier concentration,  $W_0$  and  $W_f$  are the initial and final depletion depths,  $W$  is the depth at which  $T_c$  is calculated, and  $C_{ox}$  is the oxide capacitance. For an SOS film neither  $N_B$  nor  $\tau$  are uniform, and when depletion extends to the silicon-sapphire interface, additional charge generation and trapping centers contribute to the leakage current. Dr. Kranzer<sup>28</sup> designed gate controlled diodes (GCD's) on SOS which could be used for evaluating these parameters. He measured the gate capacitance and leakage current as a function of gate and junction bias. His results were first interpreted by a simple one-dimensional model<sup>26</sup> and later by a two-dimensional numerical analysis developed in the contractual work.<sup>13,29</sup> Figures 8 and 9 illustrate experimental and computed results. The method for calculation is described in reference 29.

The analytical interpretation of the data is that the lifetime and doping vary through the silicon film. At the silicon-sapphire interface, there are surface states; most of these are shallow states and cause an accumulation of free carriers. Depending upon the surface state density,  $Q_{ss1}$ , the film may or may not deplete before inversion occurs at the silicon-SiO<sub>2</sub> interface, as evidenced by the

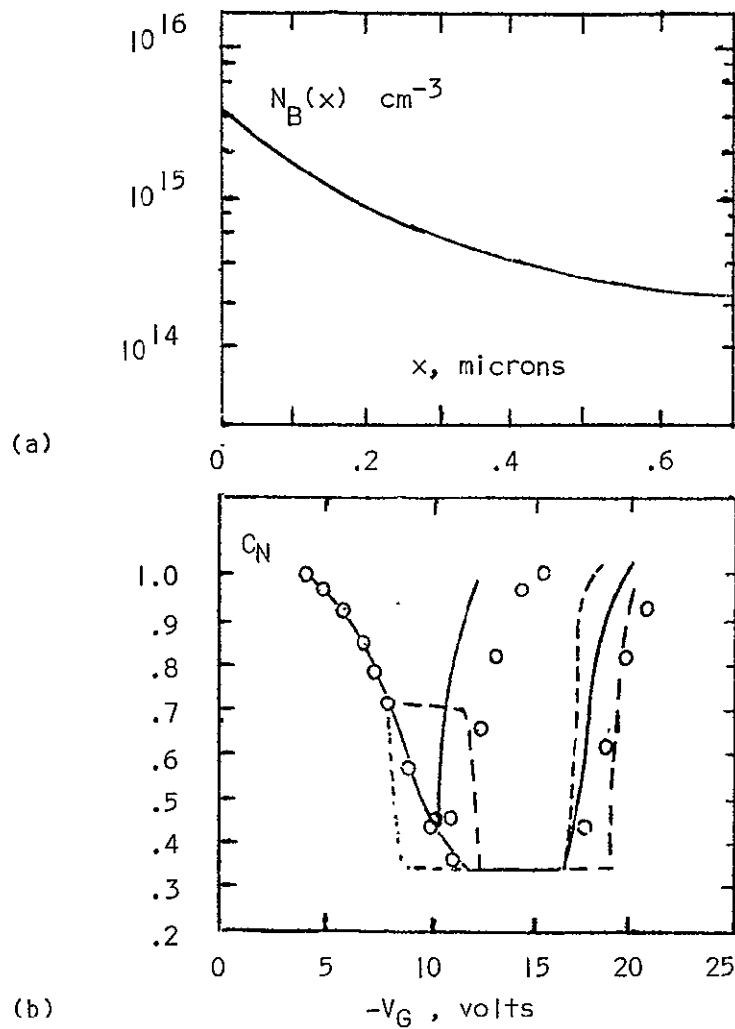


FIGURE 8

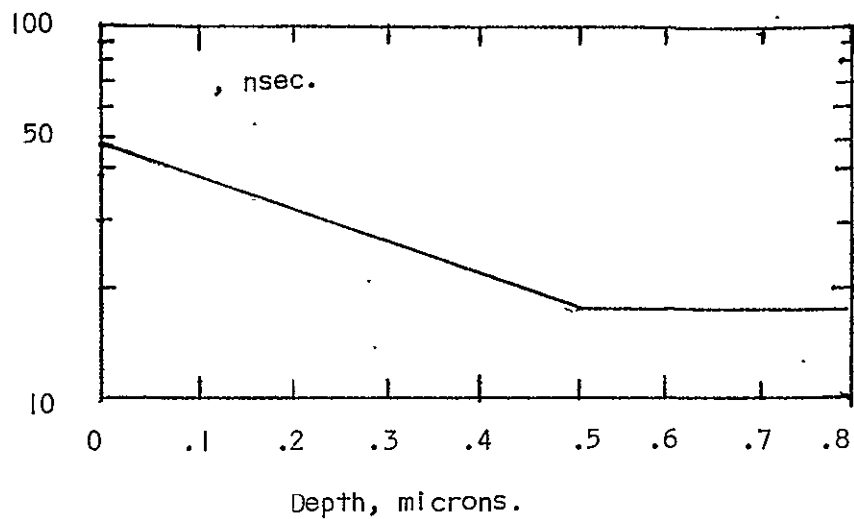
Gate capacitance vs. gate bias voltage.

Dotted:  $Q_{SS1}/q = 7.5 \times 10^9 \text{ cm}^{-2}$ , uniform distribution.

Dashed:  $Q_{SS1}/q = 1.25 \times 10^{11} \text{ cm}^{-2}$ , uniform distribution.

Solid: Exponential distribution between above endpoints.

Assumed background doping shown in (a) above. Other parameters are silicon film thickness of 0.8 microns, oxide thickness of 0.4 microns,  $Q_{SS2}/q = 2.1 \times 10^{11} \text{ cm}^{-2}$ .



(a) Assumed lifetime distribution in film. Surface recombination velocity is assumed to be 5640 cm/sec.

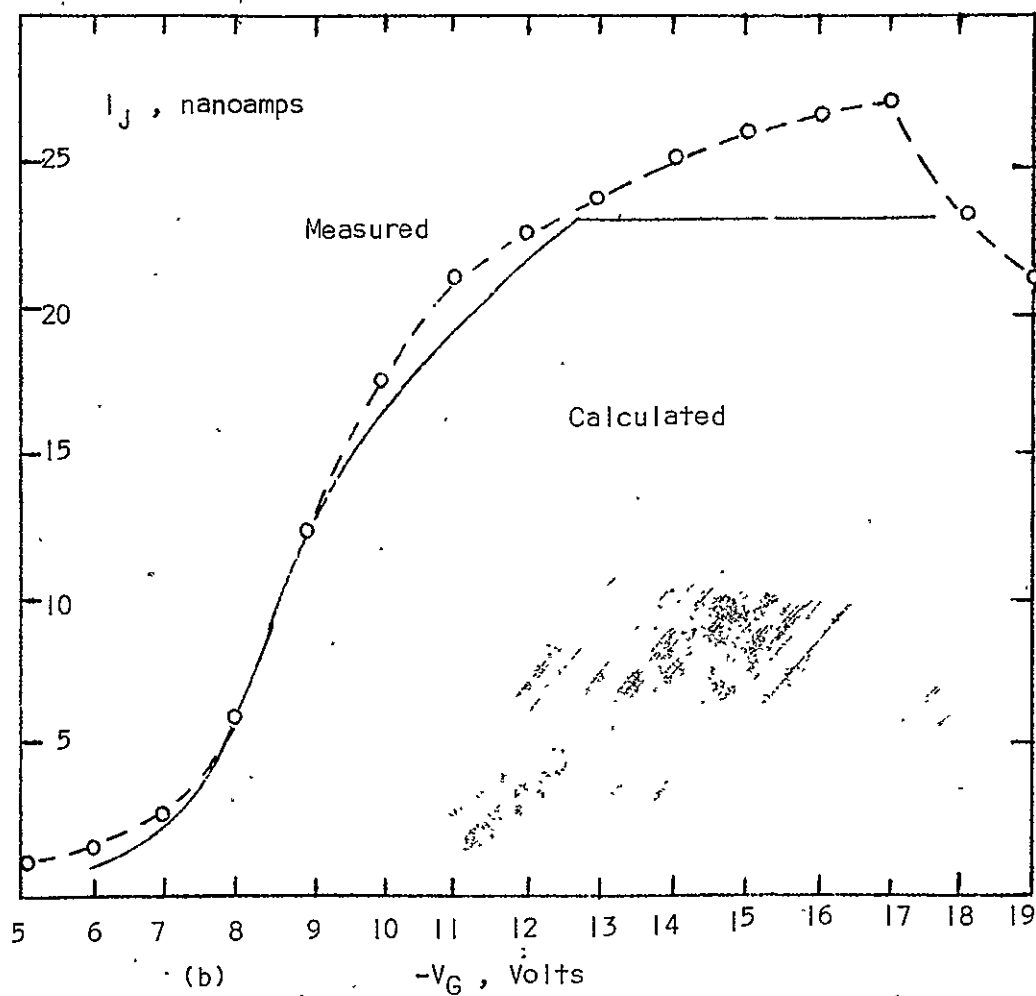


FIGURE 9

Junction current vs. gate bias in volts.



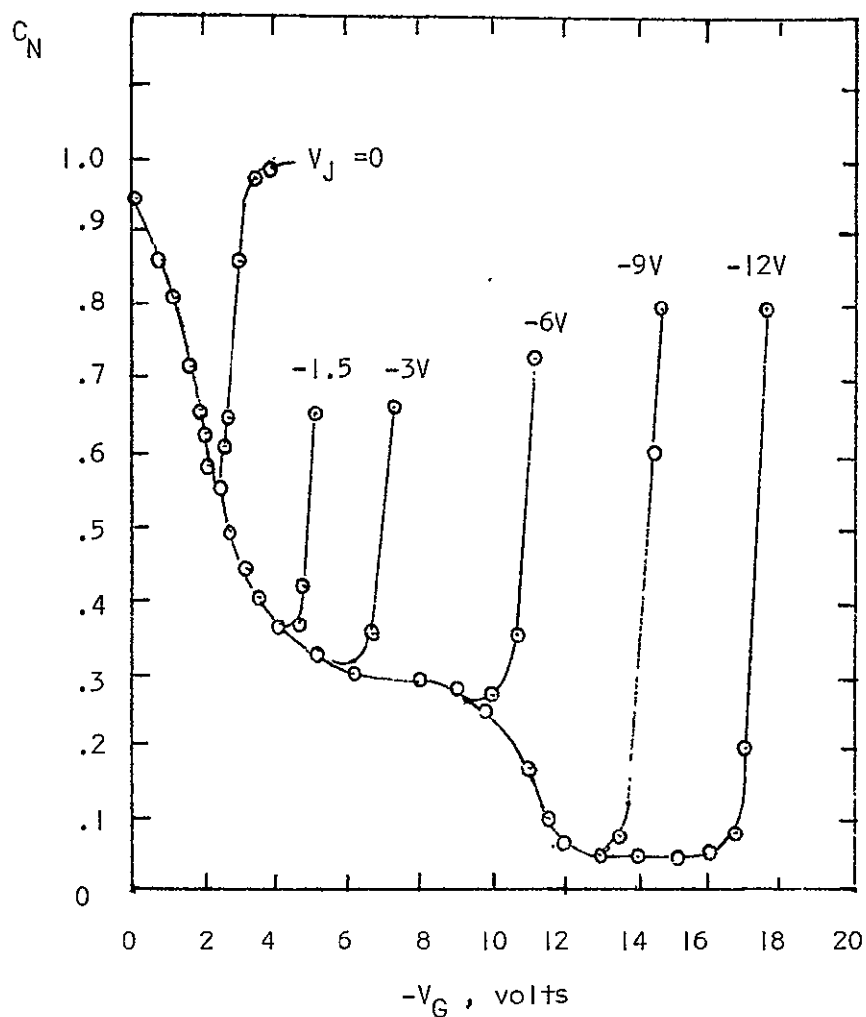


FIGURE 10

Normalized capacitance vs. gate voltage for GCD on SOS with 2 micron thick film. Unpublished experimental results by Kranzer. Note offset similar to theoretical dashed curve in Figure 8 where charge at Si-Sapph. interface prevents through depletion.

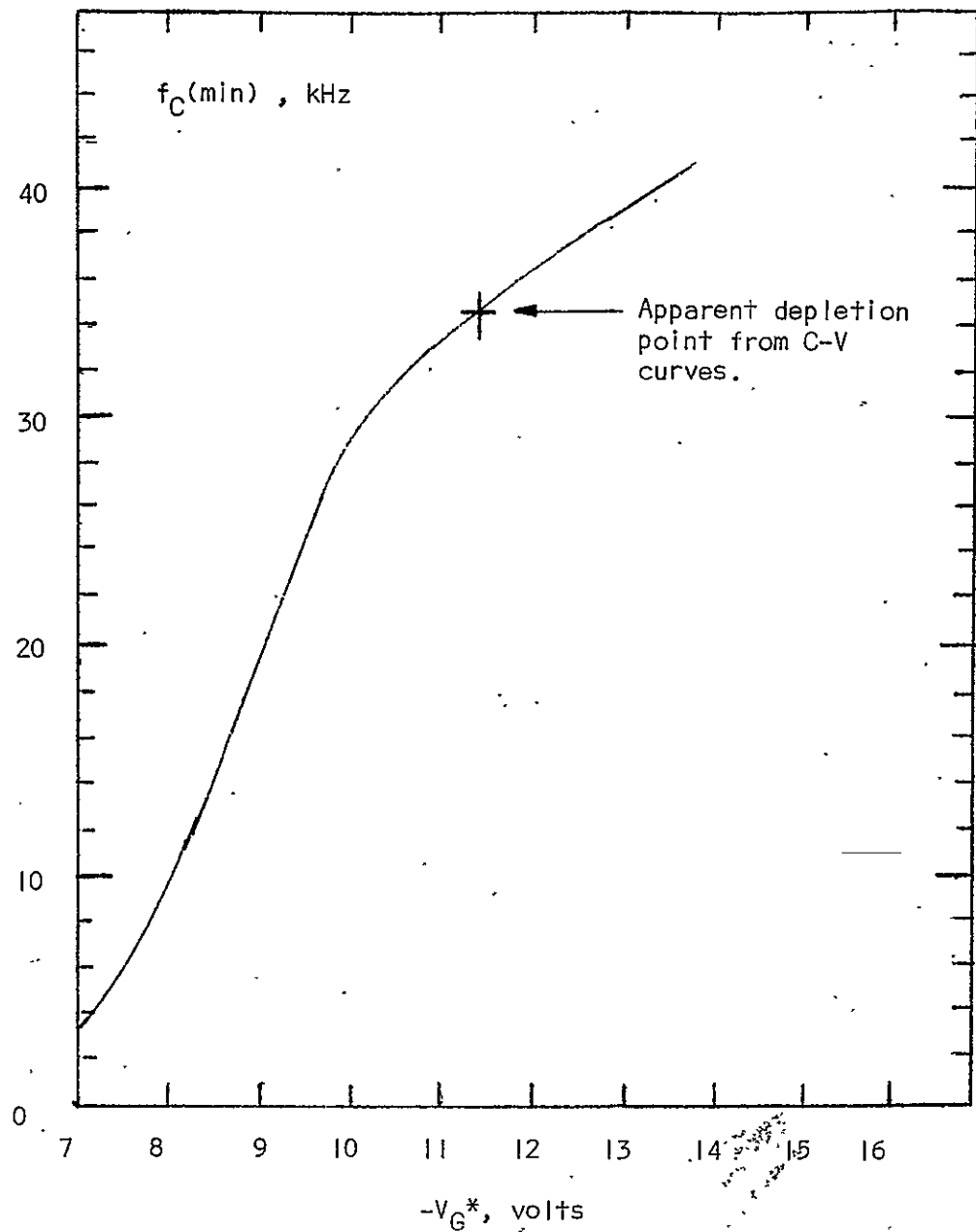


FIGURE 11

Minimum frequency for 2 micron film on the basis of Kranzer's leakage current for 1 micron film.  
 \* The true  $V_G$  for 2 micron film would be scaled up and shifted to the right.

rising C - V curve at higher gate voltages. Figure 10 shows experimental curves which show first depletion and then penetration of the field into the sapphire. The similarity with the calculated curves in Figure 8 is obvious. After the film is depleted, the surface states participate in the capture and release of free carriers so that the leakage current rises after the capacitance saturates. Finally, as inversion sets in, a shielding effect at the Si - SiO<sub>2</sub> interface, which becomes an equipotential plane, results in a slight decrease in leakage current. The gate capacitance increases in the manner expected.

Figure 11 utilizes Dr. Kranzer's leakage current data placed on a unit area basis to calculate the time required for the leakage current to increase the Si - SiO<sub>2</sub> interface potential by one volt. This time is given by:

$$\tau_c = C_{ox} \times 1 \text{ volt} / J_L \quad (5)$$

Where  $J_L$  is the per unit area leakage current which depends upon the gate bias. This time is used as a measure of the low frequency limit for the CCD on SOS. Defining  $f_c$ ,  $p$ , and  $N$  respectively as the clock frequency,\* number of phases, and number of cells in a CCD shift register, the transfer time through the register is

$\tau_T = Np / f_c$ , which must be small compared with the charge up time. Therefore:

$$f_c \gg Np J_L / C_{ox} \quad (6)$$

---

\*It is assumed, as customary, that the clock frequency is divided to obtain the phases.

Taking a  $2,000\text{\AA}$  gate, which should be conservative, the value of  $J_L$  at which the film is apparently depleted,  $P = 2$  and  $N = 32$  (for a 32 bit SR), the minimum frequency is:

$$f_c \gg 34.5 \text{ KHz} \quad (7)$$

which indicates that such a CCD on SOS is feasible, if for example an order of 10 is sufficient for the inequality. The result is discouraging for imaging application since it indicates frame rates must greatly exceed  $0.5 \text{ KHz}$  which implies that any gain of sensitivity from back side imaging may be lost due to short integration time.

The next step was to construct and test CCD's on SOS. Two-phase, polysilicon-aluminum gate CCD's were designed by Dr. Kranzer and fabricated on both bulk silicon and SOS. Film thicknesses of 1, 2, and  $6 \mu\text{m}$  were used. Three-phase gapped devices were also designed and constructed. The contractual work was responsible for designing and constructing test circuitry. The circuitry utilized TTL logic and discrete output transistors to obtain overlapping waveforms with a slower trailing edge, variable overlap and clock frequency and output amplitude. The circuitry was then used to test the CCD's.

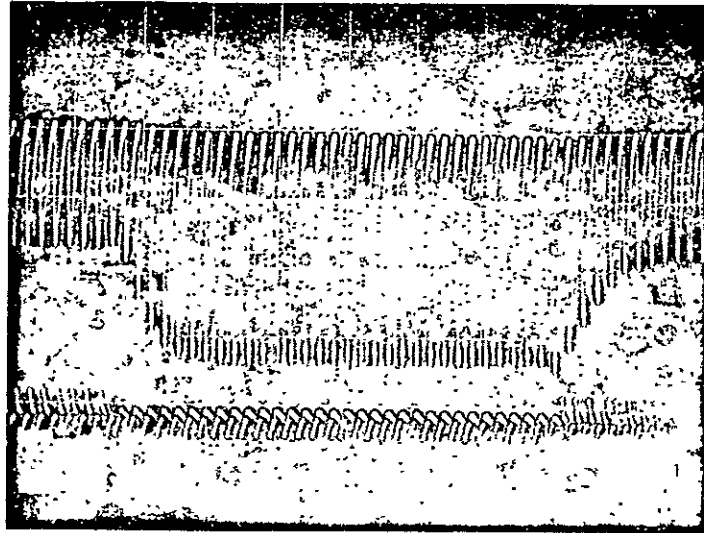
The first tests were made on a probe station which allowed a large number of devices to be tested. Most devices constructed on bulk were operational, with the two-phase devices considerably better. The only problem was with the floating output diffusion sensor and associated FET. During oxidation of the poly-silicon, hydrogen enhanced boron diffusion through the channel oxide results in an inverted channel making it more difficult to bias the output. This

was circumvented by using an output current amplifier to measure the drain current pulses. A more serious difficulty was encountered in using the probe station. Ringing created spurious output that made experimental observations almost impossible to interpret above 100KHZ. Various improvements were made, but this problem was insurmountable.

The second tests were made upon packaged two-phase devices with  $1\mu m$  film thickness and these tests are still underway. The first attempts to measure charge transfer at room temperature were negative. At frequencies up to 2 MHZ it appeared that the wells were filling with thermally generated charge. The devices were then tested at liquid nitrogen temperature and worked quite well at 100KHZ. Figure 12b shows the output for a 32 pulse train for a 32 bit SR using a fat zero. It appeared that the devices were still working at frequencies as low as 5KHZ. Leakage current checks at room and LN<sub>2</sub> temperature showed that the leakage was much reduced by cooling as was expected. However, it is not possible to duplicate the earlier tests on the GCD with a curve tracer. Curve tracer tests confirmed channel action for the CCD's. These results are somewhat puzzling, since the low temperature results and calculations indicate that the devices should work at 2MHZ (or lower.)

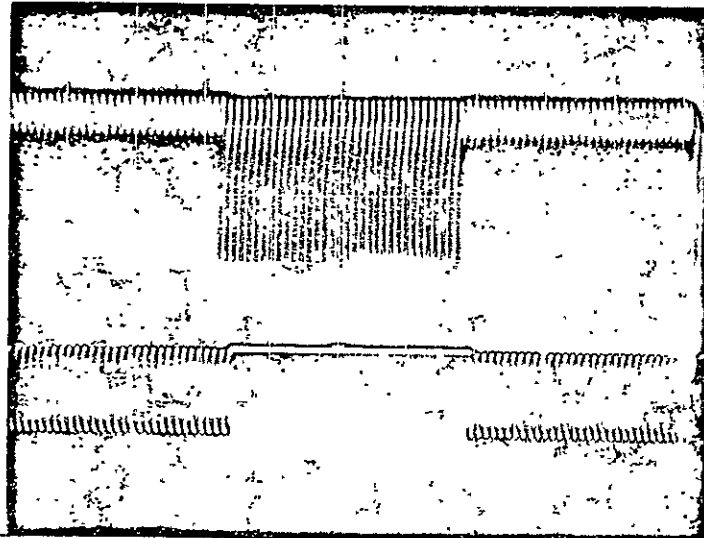
Tests at room temperature and at higher frequencies are still underway. It is also planned to obtain checks at an intermediate temperature to establish a minimum frequency vs. temperature curve. Figure 14 shows the test circuit which has been used.

The conclusions at this point are that CCD's on SOS will work even with very thin ( $1\mu m$ ) films and that cooling improves the



Vertical: 50 mV/div. Horizontal: 25 usec/div.

Figure 12-a. Device 3A charge transfer waveforms. G1 is pulsed, G2 is dc biased, ID is pulsed with gated pulse train shown on bottom trace. Substrate is grounded and no fat zero.  $\text{LN}_2$  temperature.



Vertical: 100 mV/div. Horizontal: 50 usec/div.

Figure 12-b. Device 3A charge transfer waveforms. G1 is dc biased, G2 is pulsed with gated pulse train shown on bottom trace, ID is pulsed continually, substrate bias is +3 volts, and fat zero.  $\text{LN}_2$  temperature.

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the low frequency performance. It remains to be proven that the SOS device is ultimately faster than bulk, surface channel devices, but it is reasonable to assume so unless proven otherwise. The matter of noise and transfer efficiency has not been investigated yet. It seems that the trapping-generation phenomena at the silicon-sapphire interface is complex and is difficult to evaluate experimentally. More work is needed in this area, especially on the temperature dependence of trapping. Further computer studies of the distribution in energy of these interface states would be helpful. Recent experimental results<sup>30</sup> can be used in a computer simulation of the GCD on SOS. Finally, although the results confirm that building an imaging device on SOS will be difficult, it is still conceivable that devices with low resolution and high frame rate can be fabricated and operated in a cooled mode. For ordinary applications, this would not be unsatisfactory; but for some high speed applications, these devices may be superior.

#### PHASE IV $\text{Al} - \text{Al}_2\text{O}_3$ INSULATED GATE CCD's

As previously mentioned, the advantage of this structure over the silicon-gate CCD are: (1) relatively simple low temperature process involving anodization and (2) higher conductivity gate structure. Both features are attractive for CCD's and SOS. By using ion-implantation and deposited oxides, the amount of high temperature processing for SOS is practically nil, a recognized advantage. The CCD on SOS will be a high frequency device if it is in fact viable. Therefore, the investigation of this type of gate structure was of interest.

The speed advantage of the all aluminum transfer electrode structure is best appreciated by considering an ideal RC transmission line of infinite length. The parameters of the line are  $R_s$ , the sheet resistance of the electrode structure, and  $C_s$ , the per unit area capacitance of the line. The capacitance in the analogous CCD is the channel oxide capacitance in series with the surface depletion capacitance. Although the ideal line is an obvious over simplification, it is useful to consider the worst case in which  $C_s$  is simply the oxide capacitance. The voltage response at a point X at time T on the line for a unit voltage step at X = 0 is:

$$V(x,t) = \text{erfc} \left( \sqrt{R_s C_s / t} x \right), \quad (8)$$

Where  $\text{erfc}$  is the complementary error function. The time required for the voltage to achieve half amplitude at  $X = L$  is:



$$t = R_s C L^2$$

for  $R_s = 10 \text{ ohms/sq.}$  and  $C = 3.45 \times 10^{-8} \text{ f/cm}^2$ , the time is:

$$t = 3.45 \times 10^{-7} L^2$$

A 100 cell CCD with  $10 \text{ } \mu\text{m}$  cells gives  $L = 10^{-1} \text{ cm}$  so that  $t \sim 3.45$  nanosec. which is a significant delay for 100MHZ operation. An all aluminum structure with thickness of  $5 \text{ } \overset{\circ}{\text{A}}$  and  $\rho = 2.8 \text{ } \mu\text{ohm-cm}$  results in a time shorter by a factor of 20.

The work began with evaluation of an anodization procedure which has been published and patented.<sup>14</sup> Films were anodized using a buffered tartaric acid bath with either ethylene or propylene glycol as the dilutant. Both dilutants work apparently equally well. Baseline work confirmed earlier reported relationships of approximately  $10 \overset{\circ}{\text{A}}$  per volt for the oxide thickness, which was measured by interferometry or ellipsometry. Aluminum films were both sputtered and thermally evaporated. The evaporated films have a coarser topography but appear to be more dense than sputtered films. Evaporated films on glass or bare silicon are lifted by the stresses induced by anodization. Films deposited on  $\text{SiO}_2$  do not lift, however occasional splotching due to local raising of the film is noted. Sputtered films have not been observed to lift.

During CCD fabrication, low temperature sintering of the ohmic contacts is required. It has been observed for both evaporated and sputtered films that a pebbling and pocking of the  $\text{Al}_2\text{O}_3$  occurs during sintering. The reason for this is not understood at this time

Evaporated films have been sintered prior to anodization and have appeared to be oxidized due to some contamination in the nitrogen. A cold trap was used to remove the contamination but it did not help the problem. It was later observed that the sputtered aluminum was undergoing some change in the sintering process.

A 4-phase CCD was designed and several wafers have been constructed as illustrated in the photomicrograph in Figure 12. This device utilizes dual input gates and an output circuit with a floating diffusion which can also be used as a gated charge integrator. Figure 13 illustrates these structures. A four-phase pulser was designed and constructed for testing the CCD's. Figure 14 illustrates the basic circuit which has an overlapping phase structure generated in a manner similar to an earlier reported version.<sup>14</sup>

The first devices to be fabricated were evaluated on a curve tracer to establish channel continuity and insulation integrity. They were evaluated three times over a period of four months and a progressive failure rate for the insulation integrity was noted. The design incorporated ohmic contacts on the second level of metallization which requires sintering after anodization. At this point an attempt is being made to determine if the sintering procedure is systematically connected with failure of the insulation integrity. If this is true, the design will be modified, either by change of the sequence in fabrication or the sintering ambient, etc. Afterward, CCD's will be evaluated over a period of time under conditions of stress to determine the reliability. The CCD pulser is capable of -27 volt pulses and higher D. C. biases can be used. Also test devices on

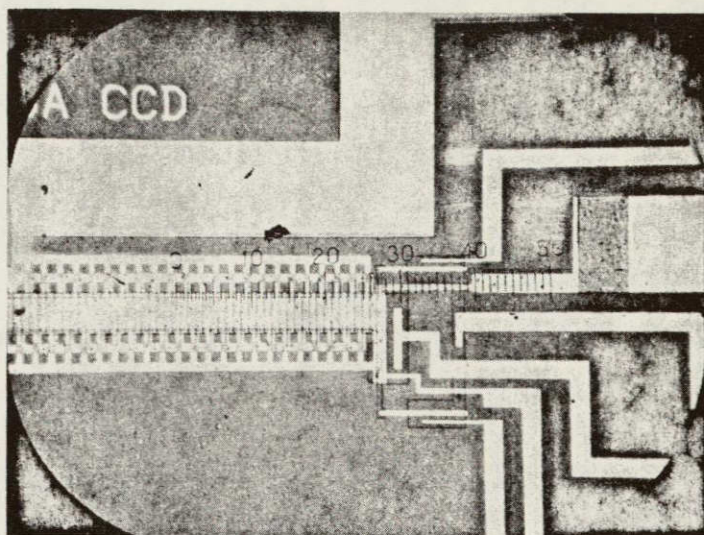


FIGURE 12

Photo Micrograph of 4-phase CCD

Showing Output Circuit

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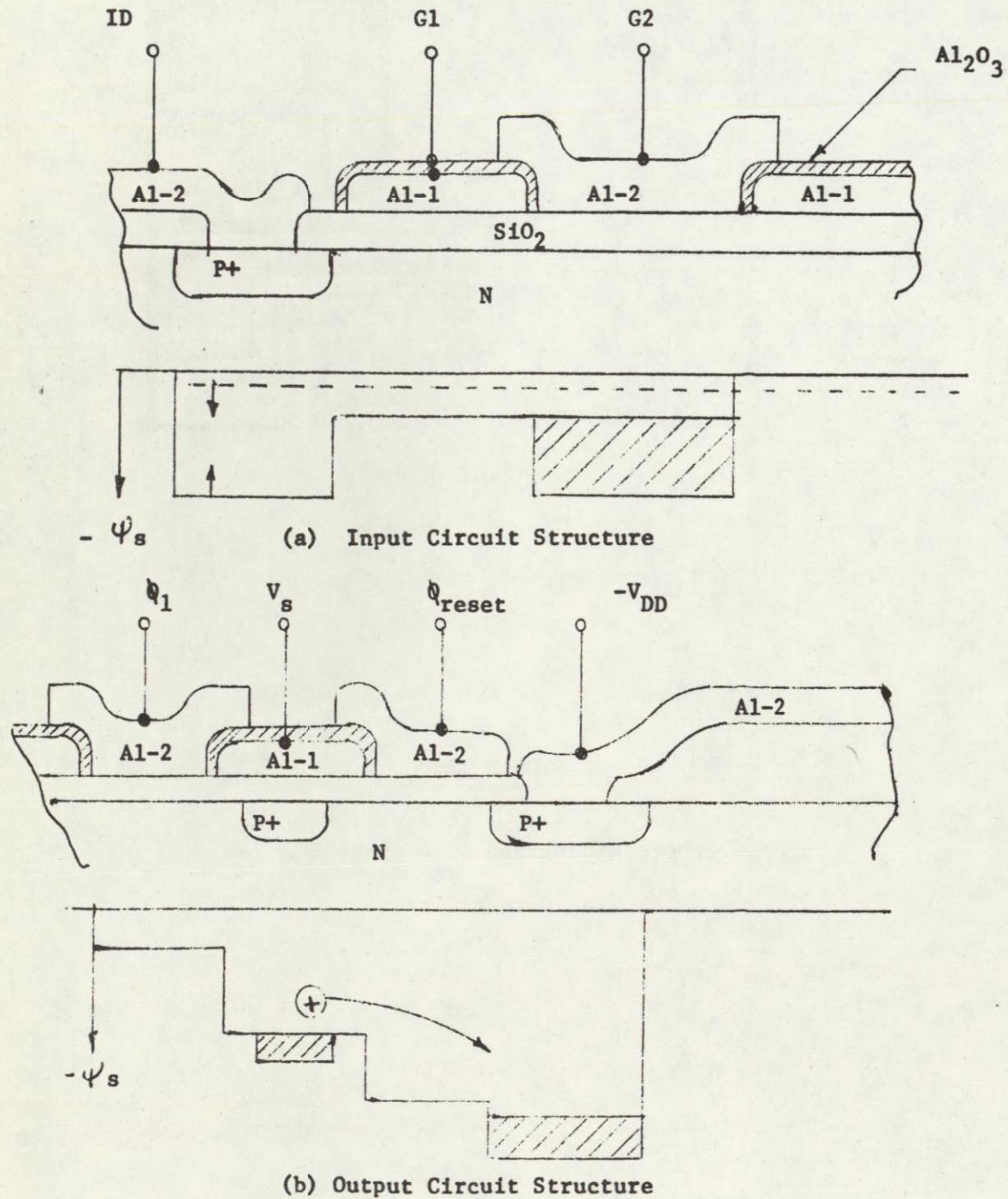


FIGURE 13

Input and output structures and surface potential profiles for 4-phase CCDs with Al- $\text{Al}_2\text{O}_3$  gate fabrication.

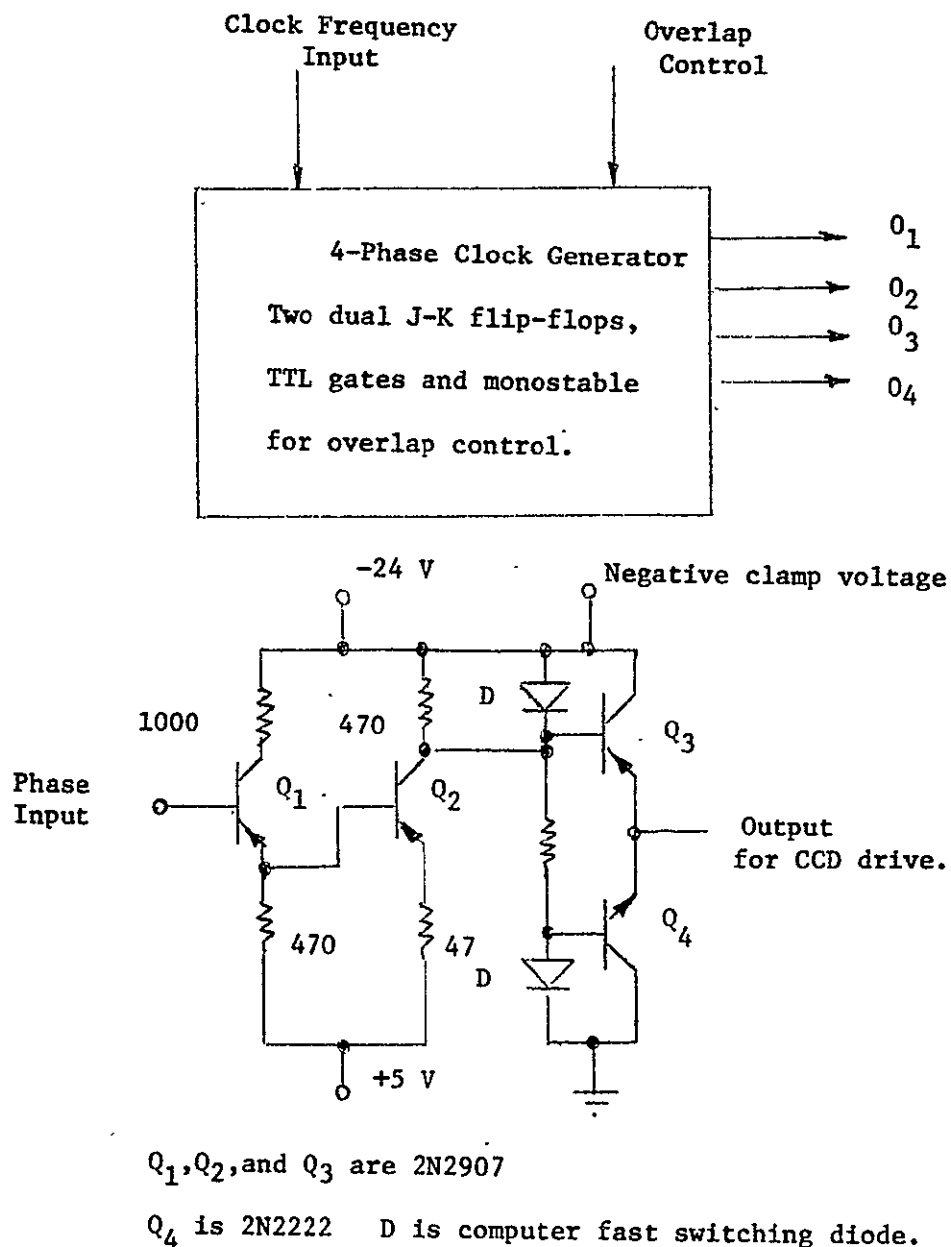


FIGURE 14

Circuits used for generating waveforms for driving CCDs.

the chip allow testing of the oxide integrity, of effects on threshold shift, etc. Elevated temperatures will also be used during the tests.

At this point, it is the conclusion that the fabrication details can be worked out and that reliable devices can be constructed. If this proves to be true, then CCD's in the future will most likely utilize this type of construction, with the possible exception of imaging devices.

#### PHASE V RELATED WORK: SOLID STATE IMAGERS<sup>19</sup>

This work was supported by MICOM and involved the evaluation of solid state imaging devices commercially available. These devices included the Reticon Camera which includes an MOS transistor-diode sensor, the Fairchild CCD-Camera, and the General Electric CID Camera. A fourth device, a high resolution CCD camera from RCA was never made available for testing. This study included analytical work, literature review, and bench testing of devices. The conclusion from this work, as indicated earlier, is that the CCD fares very well in comparison with other devices. The CCD camera structure as implemented by Fairchild has very high potential. The device tested (100 X 100 elements) had only one half the resolution of the GE CID device; however, the images were crisp and fairly free of distortion except that due to limited resolution. The device tested was not state-of-the-art with respect to blooming, and a pen light imaged in a field six feet from the camera causes complete saturation. Although markedly inferior to the CID in this regard, the modulation transfer function for the overall CCD Camera was not greatly inferior to that of the CID device with twice



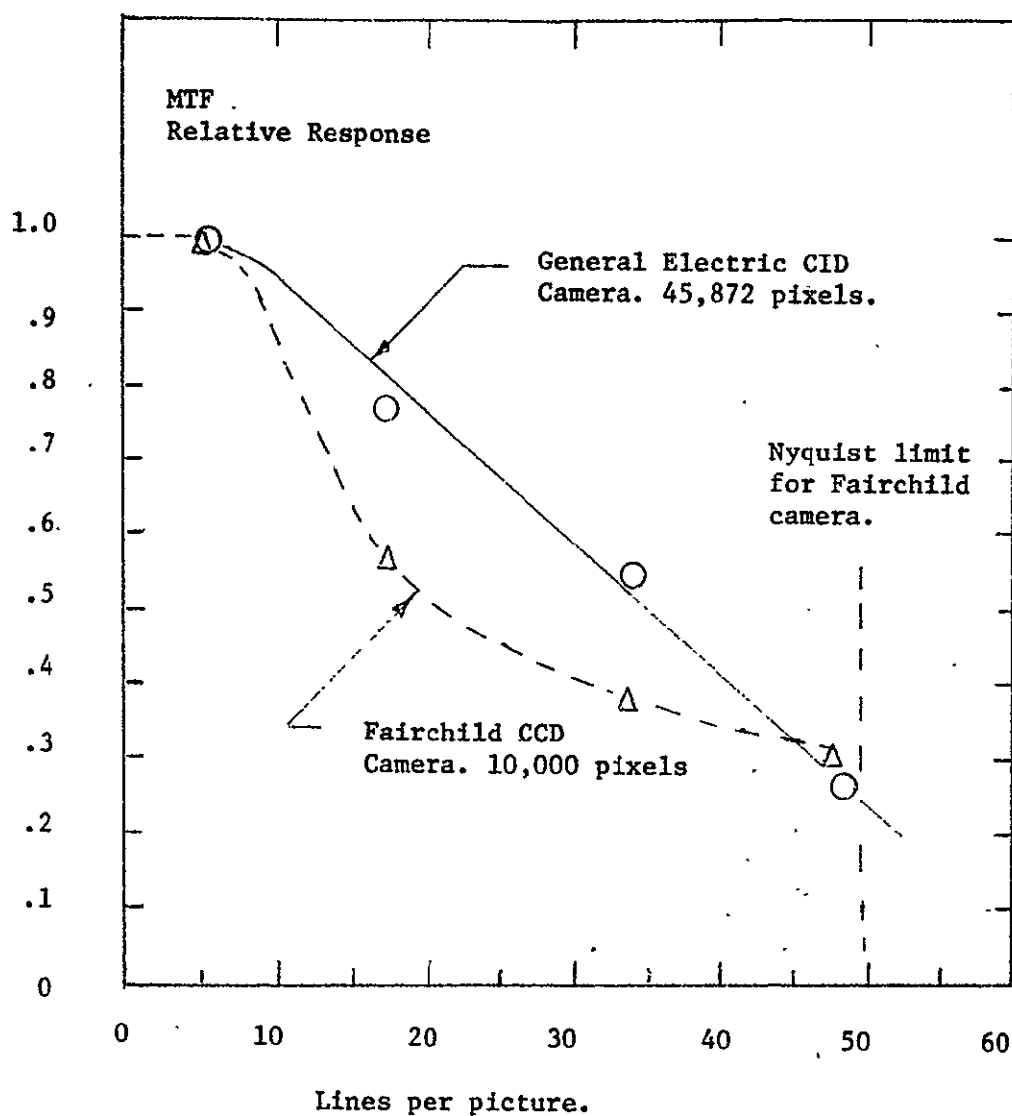


FIGURE 15

Horizontal MTF comparison for Fairchild CCD and General Electric CID cameras. Experimental results.

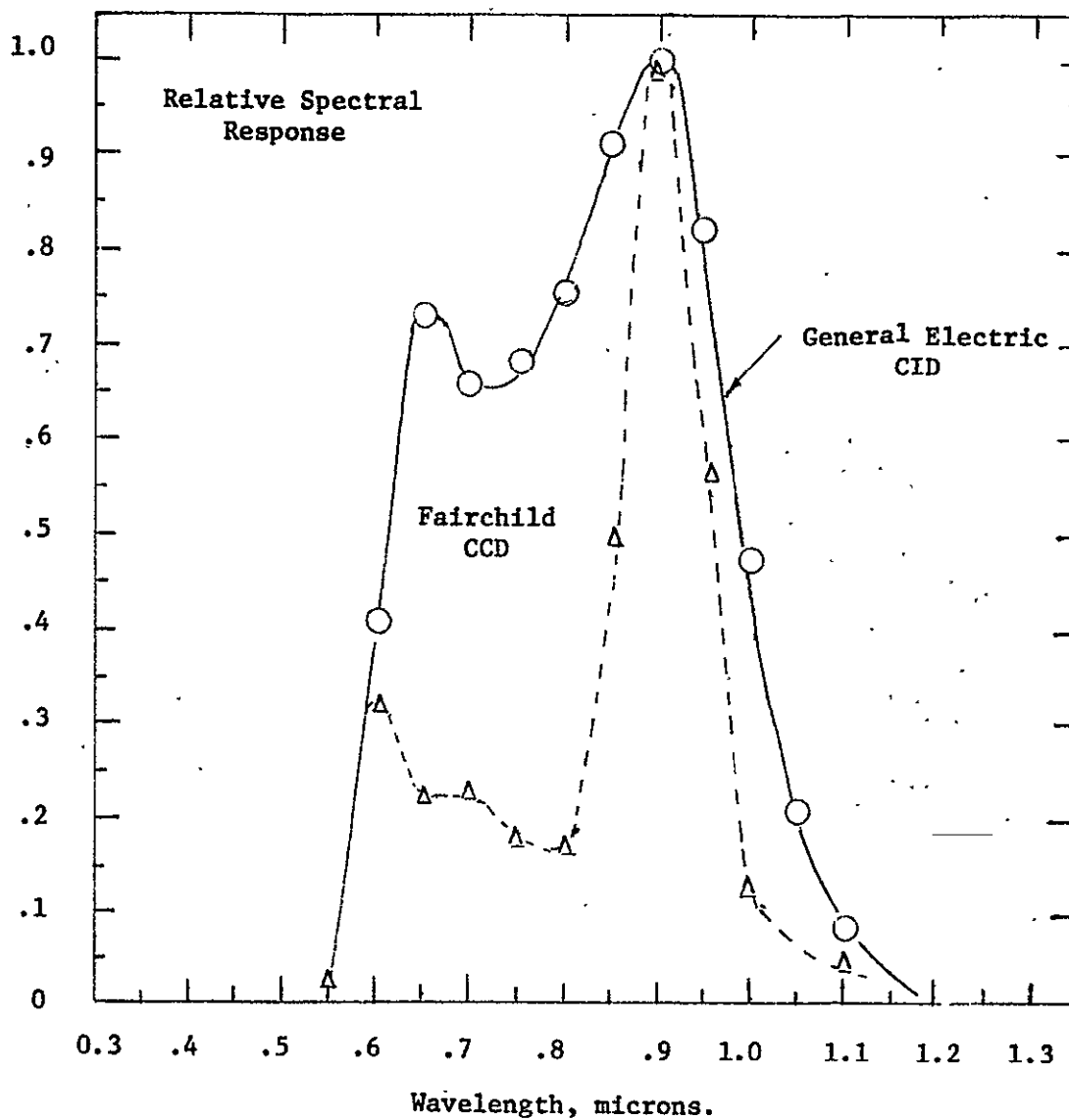


FIGURE 16

Comparison of the relative spectral responses of the Fairchild CCD and General Electric CID cameras. (Reference 19)



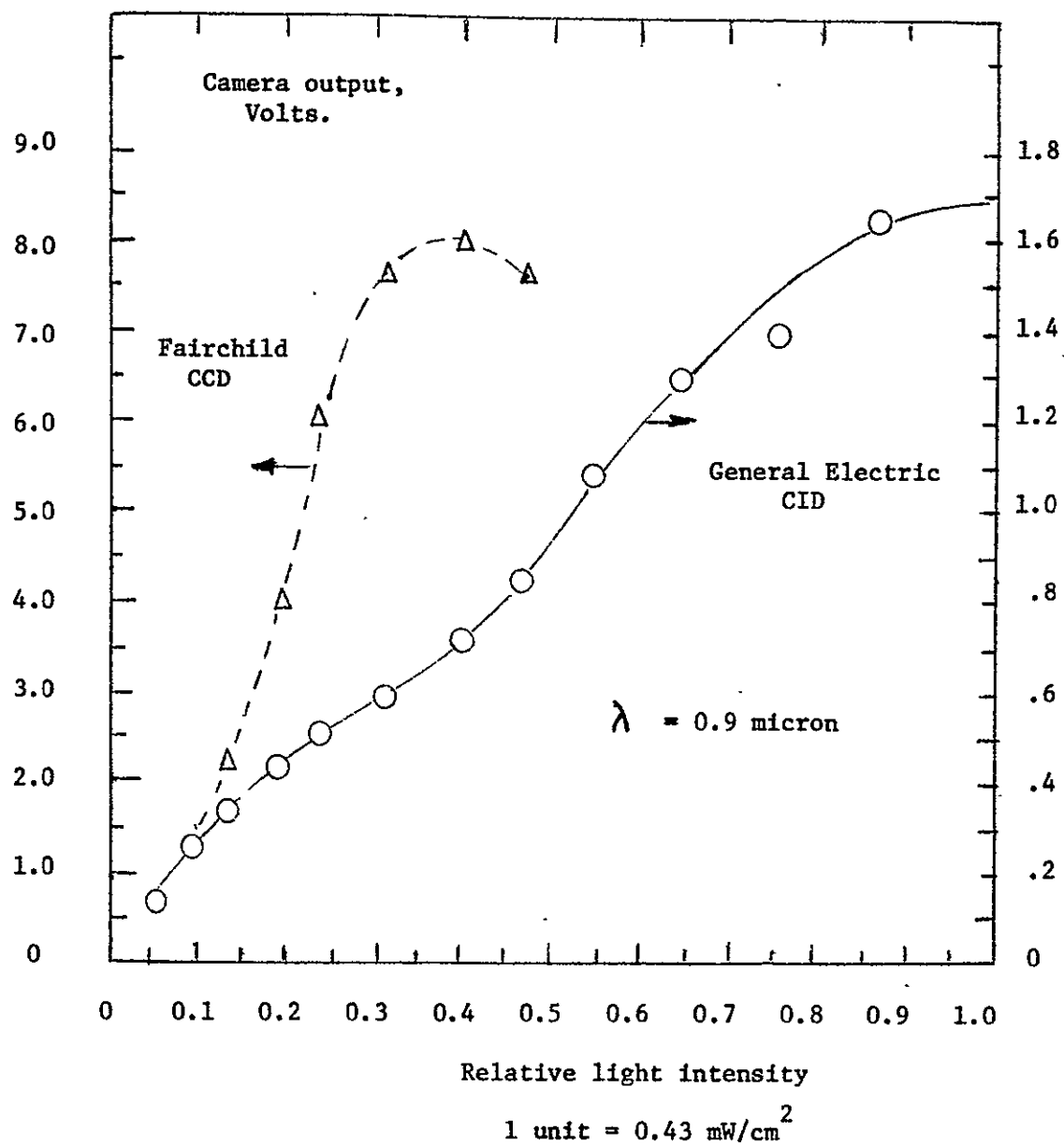


FIGURE 17

Comparison of the responsivities of the Fairchild CCD and General Electric CID cameras at 0.9 micron wavelength.

Serpentine pattern is the  
cell definition diffusion.

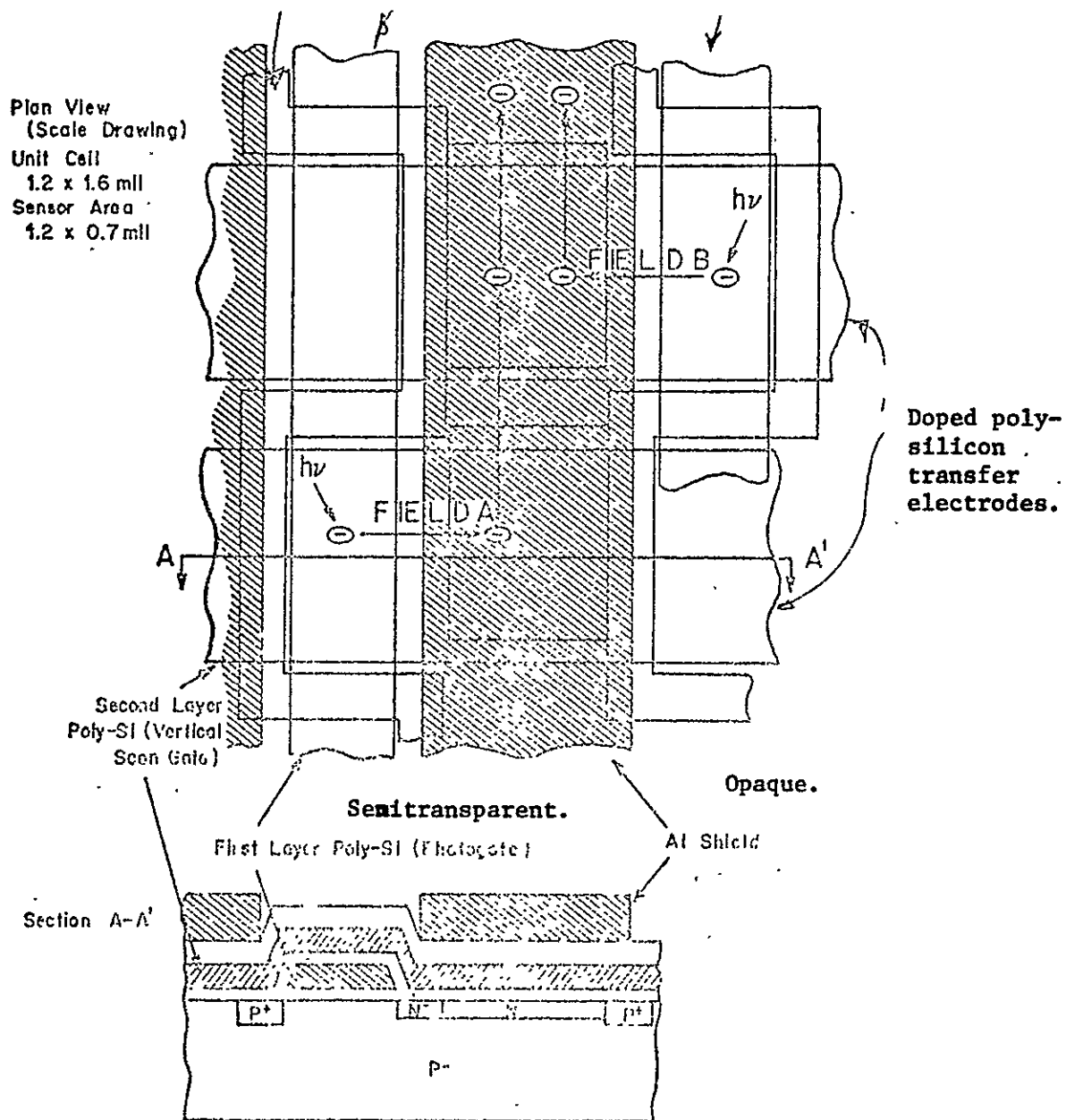


FIGURE 18

Plan view and cross-section of the unit cell of  
the Fairchild CCAID-100A image sensor device.  
(Reference 19.)

the linear (four times the area) resolution. Figure 15 compares the MTFs, Figure 16 compares the spectral selectivity, and Figure 17 the sensitivity of the two cameras. Both utilize silicon gate structures on silicon dioxide over silicon so the similarity in spectral selectivity is not surprising.

Figure 18 illustrates the construction of the Fairchild camera and several features are worth noting. First, the transfer structure is all silicon gate, and with  $10^4$  pixels and a frame rate of 150hz the bit rate is 1.5 MHz which doesn't begin to tax the device. Second, the photocharge integrator and transfer registers are integrated within the same area. This reduces the silicon area available for photon collection, yet the CCD is more sensitive than the CID. Of course, both devices suffer attenuation through the silicon gate structure. Third, the shift register structure is opaque so that photons are not being collected during transfer. The transfer from the photogate to the SR is a parallel operation and is obtained very fast. Therefore, this type design prevents smearing due to simultaneous collection and transfer. Finally, it should be noted that the overall design results in fewer charge transfers in obtaining the serial output than schemes using separate areas for photocharge integration and frame storage, i.e. such as RCA and BTL cameras. It is particularly noteworthy that the high speed transfer to frame storage is avoided with the associated reduction in charge transfer efficiency and some inevitable smearing. It has been noted that such schemes produce an obvious shading in the picture due to the increased attenuation in the MTF for field locations requiring more charge transfers.

The relative merits of the various CCD and CID imaging schemes have been debated for some time; however, the performance of devices in bench testing indicate at this time that the Fairchild concept for the CCD imager is superior. How it will ultimately fare in comparison with the GE CID is not clear at this time. Any new efforts at developing CCD imagers with new materials, such as SOS, should certainly give due consideration to the Fairchild scheme for integration of photoelements and SR structure.

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